What is claimed is:

1. A memory device comprising:

a set of memory cells to store data; and

a foot transistor coupled to the set of memory cells to provide a stack effect.

2. The memory device as set forth in claim 1,

wherein the foot transistor is ON during a read operation on one of the memory cells, and wherein the foot transistor is OFF when no read operation is performed on any of the memory cells.

3. The memory device as set forth in claim 2, wherein each memory cell comprises:

a read-access transistor;

a read-select port to turn the read-access transistor ON during a read operation; and

a read-pass transistor to provide a low impedance path between the read-access transistor and the foot transistor if the memory cell stores a first logical state, and to provide a high impedance path between the read-access transistor and the foot transistor if the memory cell stores a second logical state;

wherein the foot transistor and the read-access transistor provide a stack effect if the memory cell stores the first logical state and the read-access transistor and the foot transistor are OFF; and

wherein the foot transistor and the read-pass transistor provide a stack effect if the memory cell stores the second logical state and the foot transistor is OFF.

5. The memory device as set forth in claim 3, further comprising:

a bit line to read the data stored in the set of memory cells; and

a pullup transistor to pull the bit line HIGH if ON, wherein the pullup transistor is OFF during a read operation on one of the memory cells.

6. The memory device as set forth in claim 1, wherein each memory cell comprises:

a read-access transistor;

a read-select port to turn the read-access transistor ON during a read operation; and

a read-pass transistor to provide a low impedance path between the read-access transistor and the foot transistor if the memory cell stores a first logical state, and to provide a high impedance path between the read-access transistor and the foot transistor if the memory cell stores a second logical state;

wherein the foot transistor and the read-access transistor provide a stack effect if the memory cell stores the first logical state and the read-access transistor and the foot transistor are OFF; and

wherein the foot transistor and the read-pass transistor provide a stack effect if the memory cell stores the second logical state and the foot transistor is OFF.

7. The memory device as set forth in claim ~~6~~, further comprising:

a bit line to read the data stored in the set of memory cells; and

a pullup transistor to pull the bit line HIGH if ON, wherein the pullup transistor is OFF during a read operation on one of the memory cells.

8. A memory device, the memory device comprising:

a bit line;

a set of memory cells, each memory cell comprising:

a read-pass transistor having a source and a drain;

a read-select transistor having a drain connected to the bit line and a source connected to the drain of the read-pass transistor; and

a foot transistor having a drain connected to the source of each read-pass transistor;

wherein the foot transistor is ON during a read operation on one of the memory cells, and wherein the foot transistor is OFF when there is no read operation on any of the memory cells.

9. The memory device as set forth in claim 8, further comprising:

a pullup pMOSFET to pull the bit line HIGH if ON, wherein the pullup pMOSFET is OFF during a read operation on one of the memory cells.

10. The memory device as set forth in claim 9, the memory device having an evaluation phase and a pre-charge phase such that a read operation is performed only during an evaluation phase, the memory device further comprising:

a domino gate to turn OFF all the read-select transistors during a pre-charge phase, and during an evaluation phase to turn ON a read-select transistor if a read operation is performed on its memory cell.

11. The memory device as set forth in claim 8, the memory device having an evaluation phase and a pre-charge phase such that a read operation is performed only during an evaluation phase, the memory device further comprising:

a domino gate to turn OFF all the read-select transistors during a pre-charge phase, and during an evaluation phase to turn ON a read-select transistor if a read operation is performed on its memory cell.

12. A memory device comprising:

a plurality of memory cells, each memory cell comprising a read-pass transistor having a source and a drain, and comprising a read-access transistor having a drain and having a source connected to the drain of the read-pass transistor; where the plurality of memory cells are grouped into sets of memory cells, where each set of memory cells is grouped into subsets of memory cells; and

a plurality of foot transistors in one-to-one correspondence with the subsets of memory cells, each foot transistor having a drain connected to the source of each read-pass transistor in the corresponding subset of memory cells;

wherein during a read operation on a particular memory cell belonging to a particular subset of memory cells belonging to a particular set of memory cells, the foot transistor connected to the read-pass transistors in the particular subset of memory cells is

ON, where a foot transistor is OFF if connected to a subset of memory cells in which no read operation is performed.

13. The memory device as set forth in claim 12, further comprising:

a plurality of local bit lines in one-to-one correspondence with the sets of memory cells, where each local bit line is connected to the drain of each read-access transistor belonging to the corresponding set of memory cells; and

a plurality of pullup transistors in one-to-one correspondence with the local bit lines, each pullup transistor having a drain connected to the corresponding local bit line;

wherein during a read operation, the pullup transistor connected to the local bit line corresponding to the particular set of memory cells is OFF.

14. The memory device as set forth in claim 13, the memory device having an evaluation phase and a pre-charge phase such that a read operation is performed only during an evaluation phase, the memory device further comprising:

a domino gate to turn OFF all the read-select transistors during a pre-charge phase, and during an evaluation phase to turn ON a read-select transistor if a read operation is performed on its memory cell.

15. The memory device as set forth in claim 12, the memory device having an evaluation phase and a pre-charge phase such that a read operation is performed only during an evaluation phase, the memory device further comprising:

a domino gate to turn OFF all the read-select transistors during a pre-charge phase, and during an evaluation phase to turn ON a read-select transistor if a read operation is performed on its memory cell.

16. A memory device to read stored data addressable by an n-bit address, the memory device comprising:

a plurality of 2^n memory cells, each memory cell comprising a read-pass transistor having a source and a drain, and comprising a read-access transistor having a drain and having a source connected to the drain of the read-pass transistor; where the plurality of 2^n memory cells are grouped into 2^m sets of 2^{n-m} memory cells, where $0 \le m \le n$, where each set of 2^{n-m} memory cells is grouped into 2^k subsets of memory cells so that there are 2^{m+k} subsets of memory cells, where $0 \le k \le n-m$, each subset of memory cells having 2^{n-m-k} memory cells;

a plurality of 2^{m+k} foot transistors in one-to-one correspondence with the 2^{m+k} subsets of memory cells, each foot transistor having a drain connected to the source of each read-pass transistor in the corresponding subset of memory cells; and

a decoder coupled to the pluralities of memory cells and foot transistors, such that during a read operation on a particular memory cell belonging to a particular subset of 2^{n-m-k} memory cells belonging to a particular set of 2^{n-m} memory cells, the foot transistor connected to read-pass transistors in the particular subset of 2^{n-m-k} memory cells is ON, where a foot transistor is OFF if connected to a subset of 2^{n-m-k} memory cells in which no read operation is performed.

17. The memory device as set forth in claim 16, further comprising:

a plurality of 2^m local bit lines in one-to-one correspondence with the 2^m sets of 2^{n-m} memory cells, where each local bit line is connected to the drain of each read-access transistor belonging to the corresponding set of 2^{n-m} memory cells; and

a plurality of 2^m pullup transistors in one-to-one correspondence with the 2^m local bit lines, each pullup transistor having a drain connected to the corresponding local bit line;

wherein the decoder is coupled to the plurality of pullup transistors such that during a read operation on the particular memory cell, the pullup transistor connected to the local bit line corresponding to the particular set of 2^{n-m} memory cells is OFF.

18. The memory device as set forth in claim 17, wherein the decoder:

decodes the n bits of the n-bit address to provide 2^n read select signals in one-to-one correspondence with the plurality of memory cells so that each read select signal affects switching of the read-access transistor of the corresponding memory cell;

decodes the m most significant bits of the n-bit address to provide 2^m local bit line select signals in one-to-one correspondence with the plurality of 2^m pullup transistors so that each local bit line select signal affects switching of the corresponding pullup transistor; and

decodes the $m+k$ most significant bits of the n-bit address to provide 2^{m+k} foot transistor select signals in one-to-one correspondence with the foot transistors so that each foot transistor select signal affects switching of the corresponding foot transistor.

19. The memory device as set forth in claim 18, the memory device having an evaluation phase and a pre-charge phase where a read operation is performed during an evaluation phase, further comprising:

a domino gate to provide 2^n dynamic read select signals in one-to-one correspondence with the 2^n read select signals and the plurality of memory cells, so that each dynamic read select signal switches OFF the read-access transistor of the corresponding memory cell during a pre-charge phase, and switches ON the read-access transistor of the corresponding memory cell during an evaluation phase only if performing a read operation on the corresponding memory cell.

20. The memory device as set forth in claim 19, wherein each local bit line select signal keeps the corresponding pullup transistor ON during an evaluation phase only if no read operation is performed on the corresponding set of 2^{n-m} memory cells.

21. The memory device as set forth in claim 18, wherein the decoder comprises:

a post-decoder responsive to the 2^m local bit line select signals and the n-bit address to provide the 2^n read select signals and the 2^{m+k} foot transistor select signals.

22. The memory device as set forth in claim 16, wherein $k = 0$.